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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

	Pan et al.	Docket No.:	TI-31192
Serial No.:	09/998,606	Examiner:	Nguyen, C.
Filed:	11/30/01	Art Unit:	2811
For:	HIGH DENSITY CAPACITOR USING TOPOGRAPHIC SURFACE		

Request for Reconsideration after Final

Assistant Commissioner of Patents
Washington, DC 20231
June 9, 2003

Dear Sir:

The following remarks are offered in response to the Examiner's Office Action dated 02/10/2003. They are respectfully submitted as a full and complete response to that Action.

REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 18-22 are pending in this application.

The Examiner rejected claim 18 under 35 U.S.C. § 103(a) as being unpatentable over Vaartstra (U.S. 6,010,969) in view of Ouellet et al. (U.S. 6,268,620).

Applicant respectfully submits that claim 18 is patentable over Vaartstra in view of Ouellet as there is no disclosure or suggestion in the references of a parallel plate capacitor over a dielectric layer, wherein the parallel plate capacitor extends into and out of a plurality of recesses in the semiconductor layer. Vaartstra teaches a method of forming a film on a semiconductor device using carboxylate complexes. Fig. 1 of Vaartstra shows a memory cell in which a ferroelectric material 11 is formed between two electrodes 12 and 13. The bottom electrode 13 is formed on a silicon-containing layer 14 such as silicon dioxide. While layer 14 extends into recesses in a substrate, as shown in FIG. 1, layer 14 fills the recesses and no part of the capacitor extends into or out of the recesses. Accordingly, in contrast to the Examiner's assertion, Vaartstra does not teach a parallel plate capacitor that extends into and out of recesses in a semiconductor layer as required by the claim. Ouellet is added to teach that capacitors are used in memories and analog circuits. Therefore, Applicant respectfully submits that claim 18 and the claims dependent thereon are patentable over Vaartstra in view of Ouellet.

The Examiner rejected claims 18-20 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Takao et al. (JP 05029574 A) in view of Ouellet et al. (U.S. 6,268,620).

Applicant respectfully submits that claim 18 is patentable over Takao et al in view of Ouellet as there is no disclosure or suggestion in the references of an integrated circuit comprising a parallel plate capacitor over a dielectric layer, wherein the parallel plate capacitor extends into and out of a plurality of recesses in the semiconductor layer. Takao teaches forming a capacitor on the lower surface and side surfaces of an element forming area. However, as shown in FIGs 2b, 4 and 13, the capacitor only extends out of one trench and into another trench. A capacitor only exists where both the top and bottom electrodes are and the electrode 5 is etched such that it only extends out of one trench and into one trench. It does not extend into and out of a plurality of recesses, as required.

While prior to the etching of electrod 5, the electrodes and dielectric extend into and out of a plurality of trenches, Takao does not teach this as a final capacitor structure and does not disclose or suggest an integrated circuit (as opposed to a semiconductor wafer undergoing processing) comprising a parallel plate capacitor that extends into and out of a plurality of recesses in the semiconductor layer. Accordingly, Applicant respectfully submits that claim 18 and the claims dependent thereon are patentable over Takao in view of Ouellet.

The Examiner rejected claim 21 under 35 U.S.C. § 103(a) as being unpatentable over Takao et al. (JP 05029574 A) in view of Ouellet et al. (U.S. 6,268,620) and further in view of Huang et al. (U.S. 6,218,238).

Applicant respectfully submits that claim 21 is patentable over the references for the same reasons discussed above relative to claim 18 from which it depends.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejection and allowance of claims 18-22. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully Submitted,

Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, TX 75265
(214) 532-9348
Fax: (972) 917-4418

Jacqueline J. Garner
Reg. No. 36,144

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(PTO/SB/30 (5/2000))
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REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995. See The American Inventors Protection Act of 1999 (AIPA).

Application Number	[illegible]
Filing Date	11/30/2001
First Named Inventor	Pan
Group Art Unit	2811
Examiner Name	Nguyen, C
Attorney Docket Number	31-31692

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.
NOTE: 37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application [illegible]

1 Submission required under 37 C.F.R. § 1.114

a ☐ Previously submitted
- i. ☐ Consider the amendments(s)/reply under 37 C.F.R. § 1.116 previously filed on _____ (Any unentered amendment(s) referred to above will be entered).
- ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- iii. ☐ Other

b ☒ Enclosed
- i. ☒ Amendment/Reply
- ii. ☐ Affidavit(s)/Declaration(s)
- iii. ☐ Information Disclosure Statement (IDS)
- iv. ☐ Other _____

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2 Miscellaneous

a ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103 (c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R § 1.17 (i) required)

b ☐ Other _____

3 Fees The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

a ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to **Deposit Account No. 20-0668, Texas Instruments Incorporated.**
- i. ☒ RCE fee required under 37 C.F.R. § 1.17(e)
- ii. ☒ Extension of time fee (37 C.F.R. §§ 1.136 and 1.17)
- iii. ☐ Other _____

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b ☐ Check in the amount of $_____ enclosed

c ☐ Payment by credit card (Form PTO-2038 enclosed)

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print / Type)	Jacqueline J. Garner	Registration No. (Attorney / Agent)	38,144
Signature	[signature]	Date	6/9/03

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Box RCE, PO Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office on:

Name (Print or Type)	Jacqueline J. Garner, Reg. No. 38,144		
Signature	[signature]	Date	6/9/03

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Texas Instruments Incorporated
Facsimile: 972-917-4418
Phone: 214-532-9348

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9319 on the date shown below:

Jacqueline J. Garner, Reg. No. 36,144 June 9, 2003 Date

FACSIMILE COVER SHEET

X	FACSIMILE COVER SHEET	___	AMENDMENT (# Pages)
___	NEW APPLICATION	X	EOT 1 mth (3 Pages)
___	DECLARATION (# Pages)	___	NOTICE OF APPEAL (# Pages)
___	ASSIGNMENT (# Pages)	___	APPEAL (# Pages)
___	FORMAL DRAWINGS	___	ISSUE FEE (# Pages)
___	INFORMAL DRAWINGS	___	REPLY BRIEF (IN TRIPLICATE) (# Pages)
___	CONTINUATION APP'N (# Pages)	X	Request for Reconsideration (3 pages)
___	DIVISIONAL APP'N	X	RCE transmittal (3 pages)

NAME OF INVENTOR(S): Pan	RECEIPT DATE & SERIAL NO.: Serial No.: 09/998,606 Filing Date: 11/30/2001
TITLE OF INVENTION: High Density Capacitor	
TI FILE NO.: TI-31192 / DEPOSIT ACCT. NO.: 20-0668	
FAXED: 6/9/2003 DUE: 5/10/2003 ATTY/SECY: jjg	

Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, TX 75074